

FIG. 1

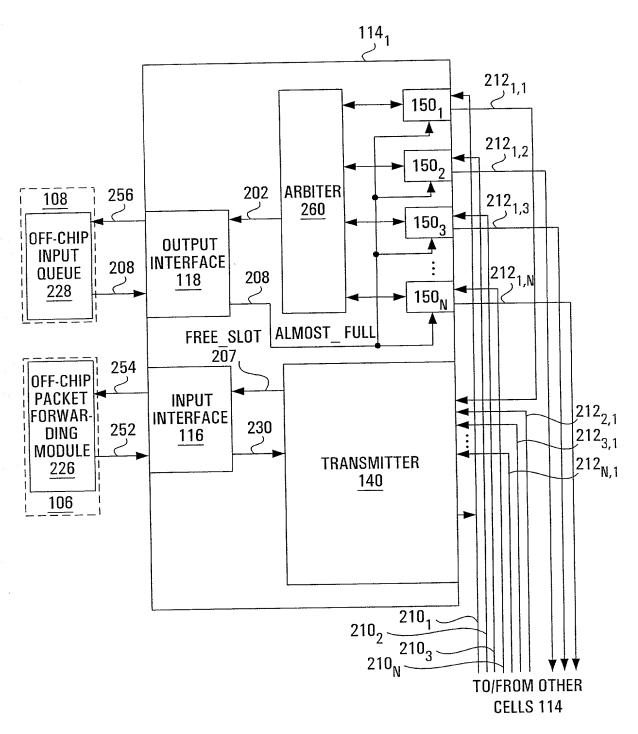


FIG. 2

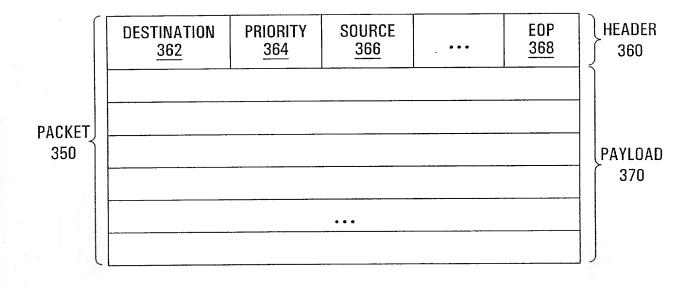


FIG. 3

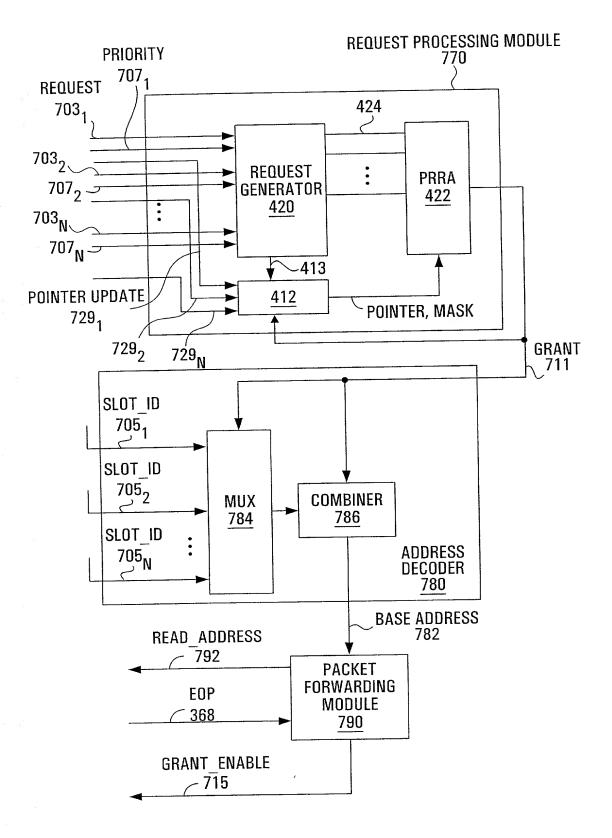
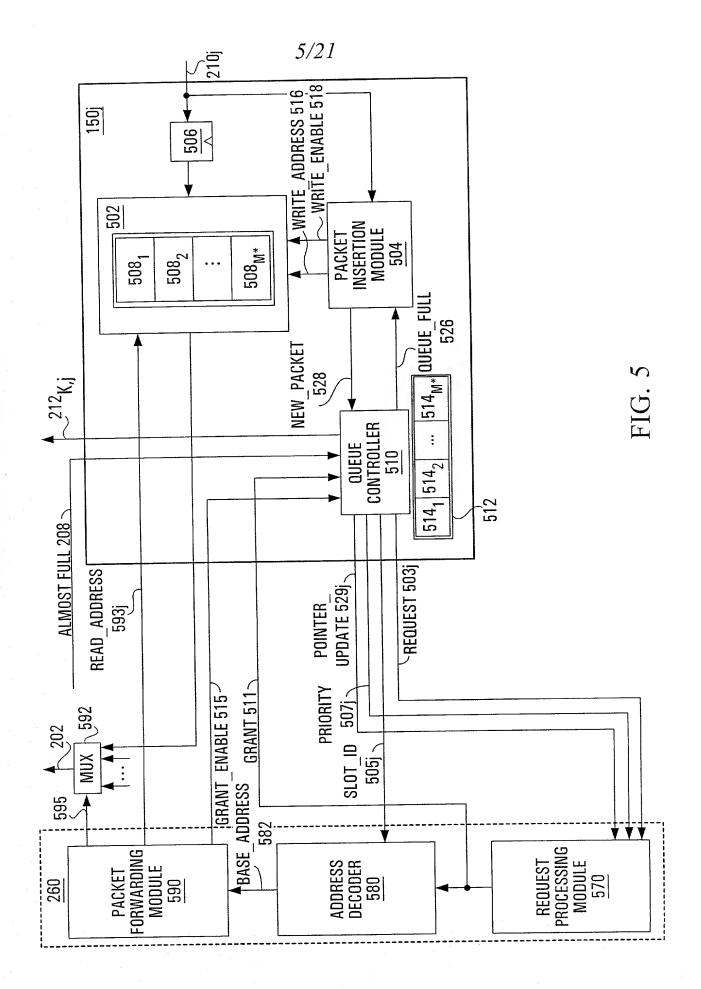


FIG. 4



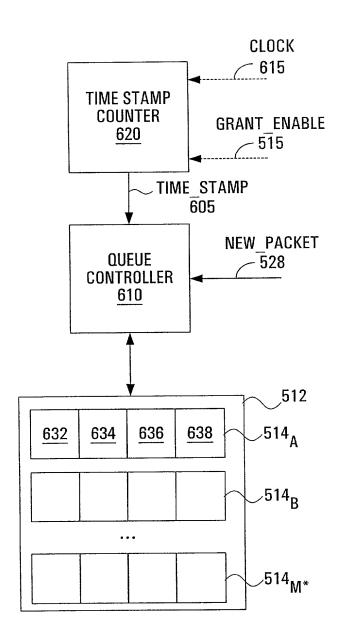
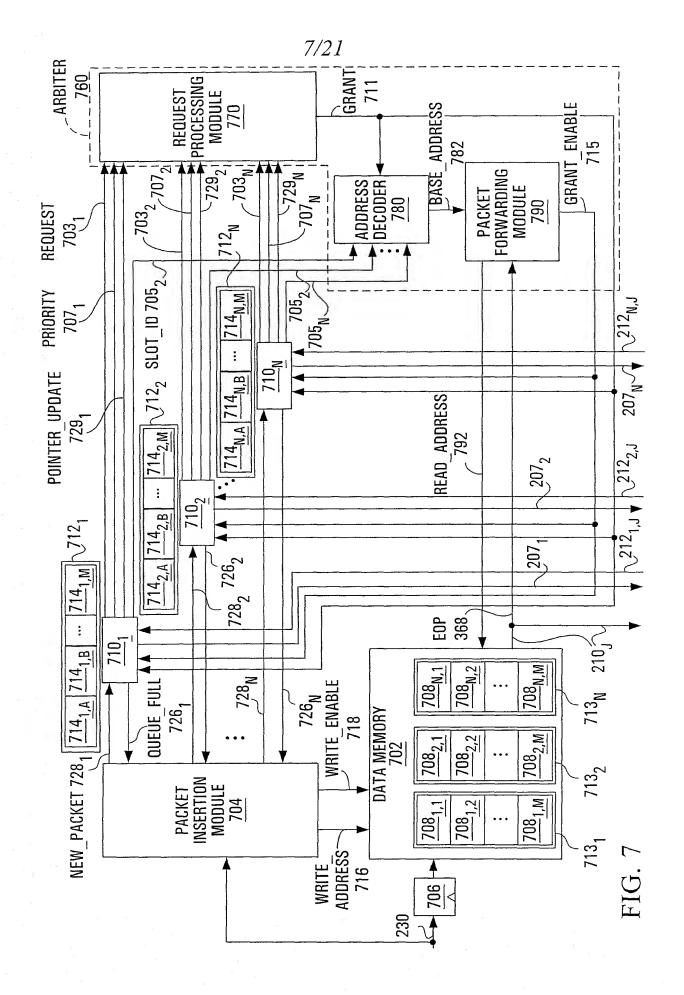
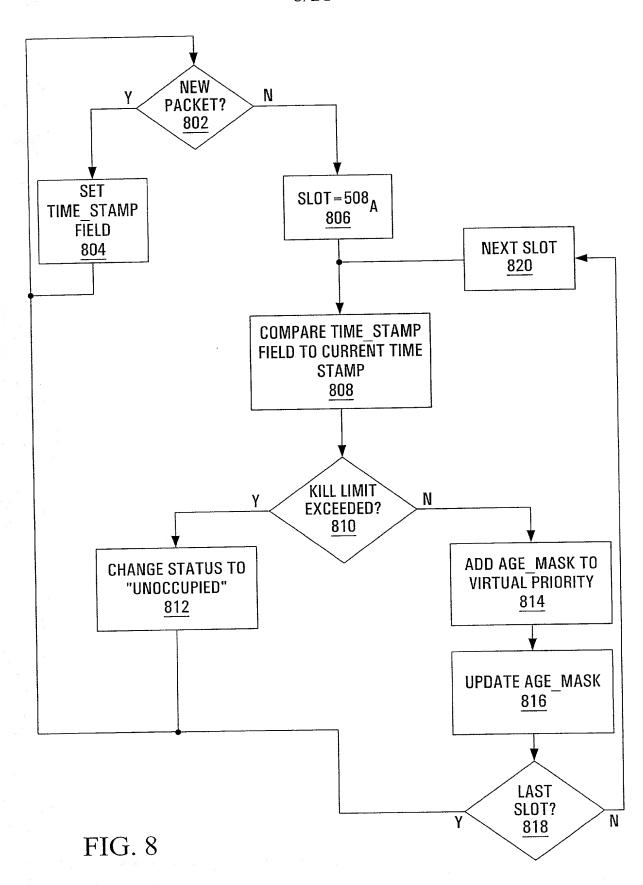


FIG. 6





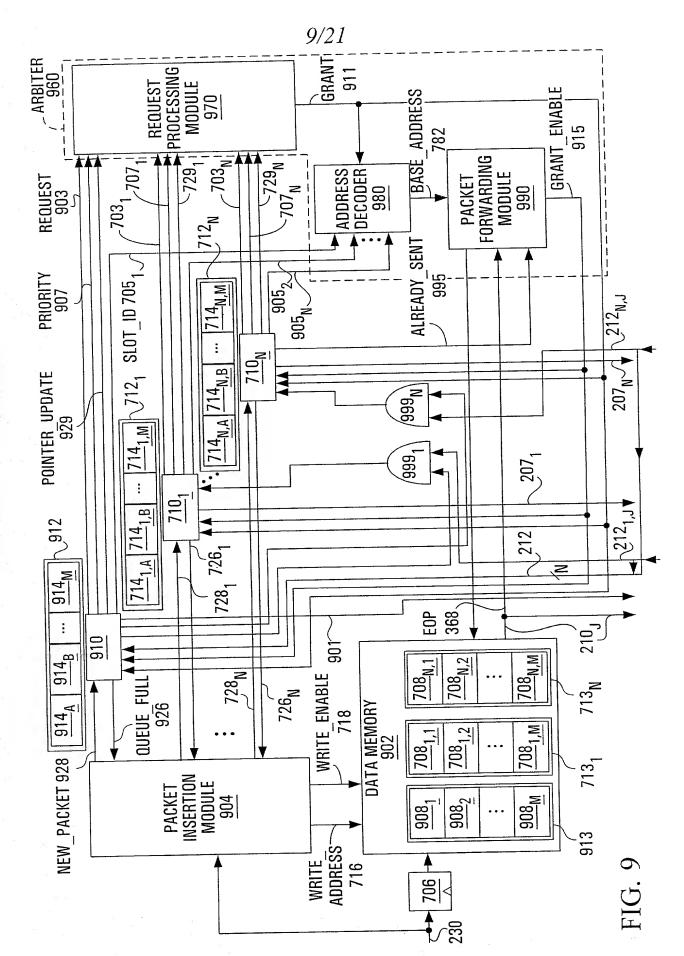


FIG. 10

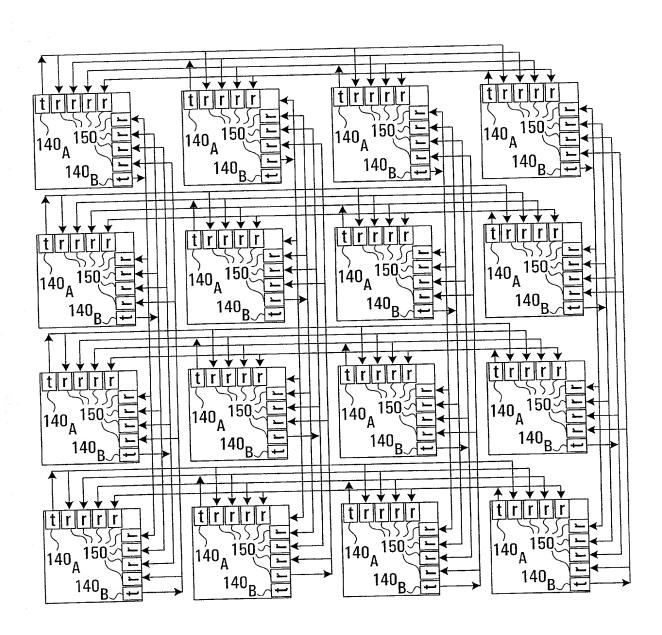


FIG. 11

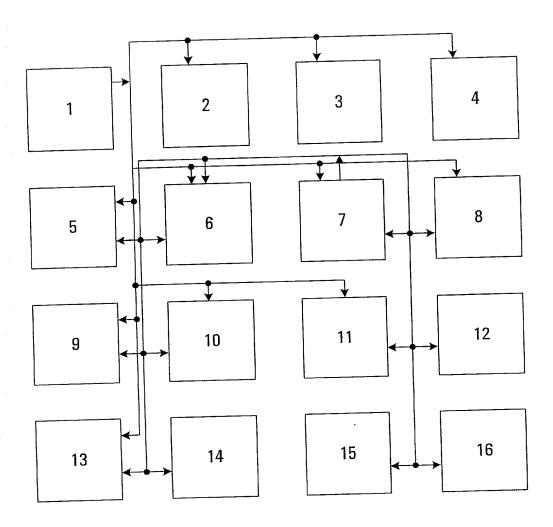


FIG. 12

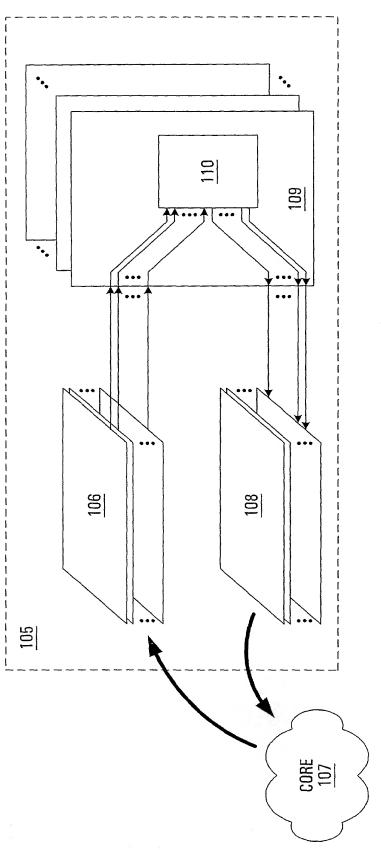
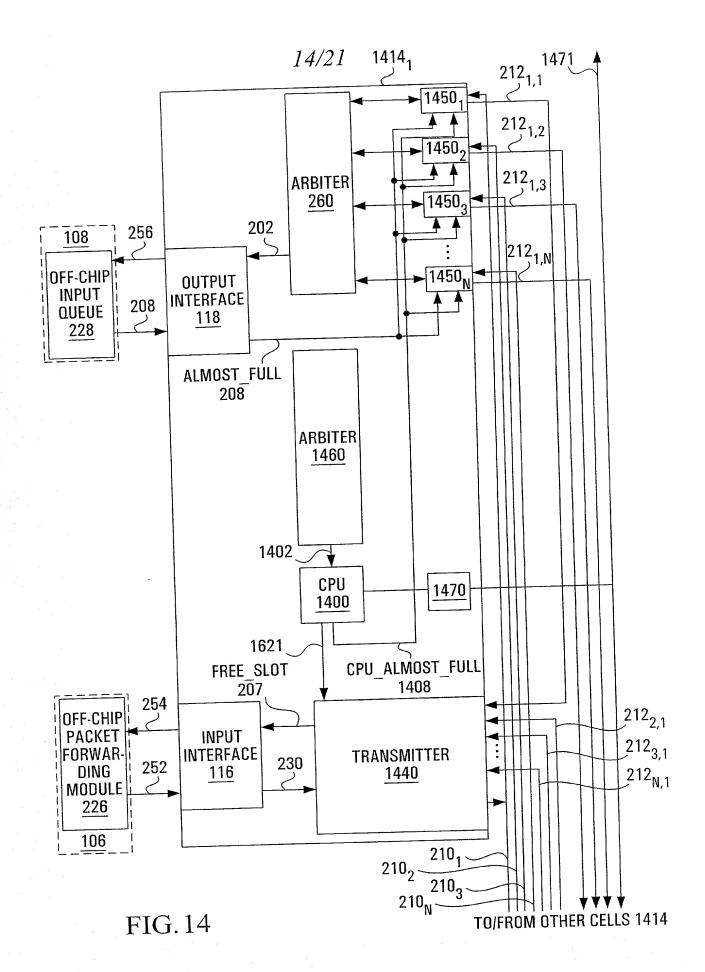


FIG. 13



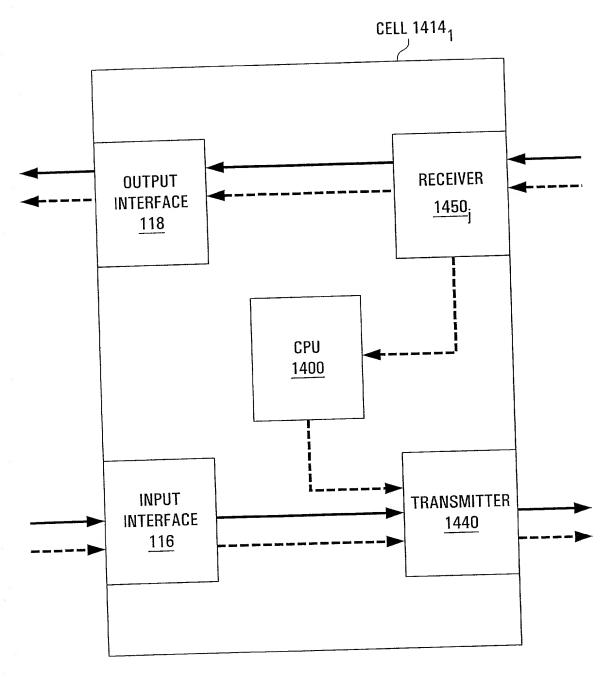
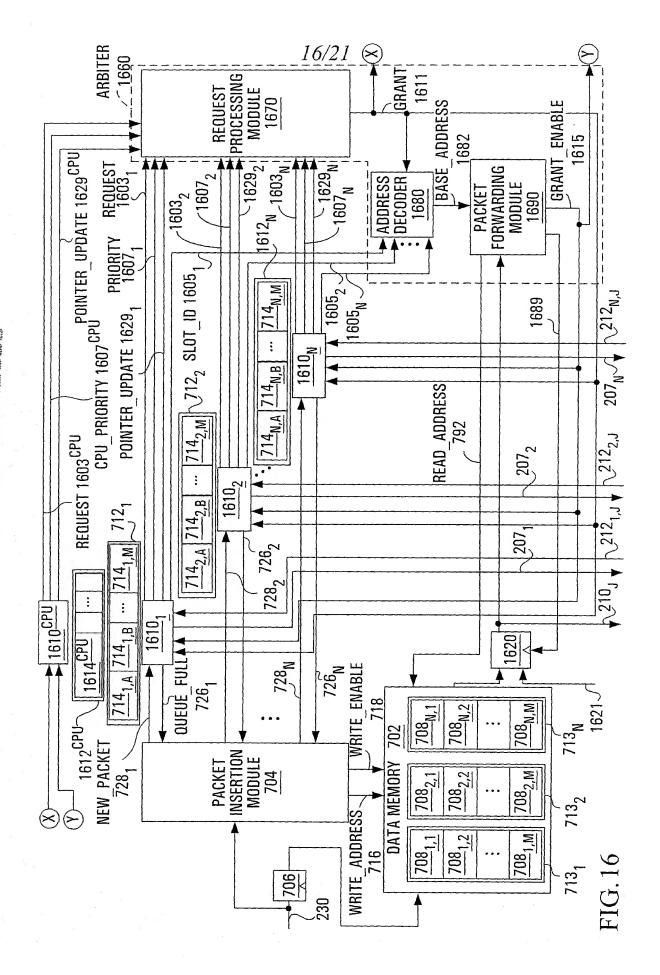


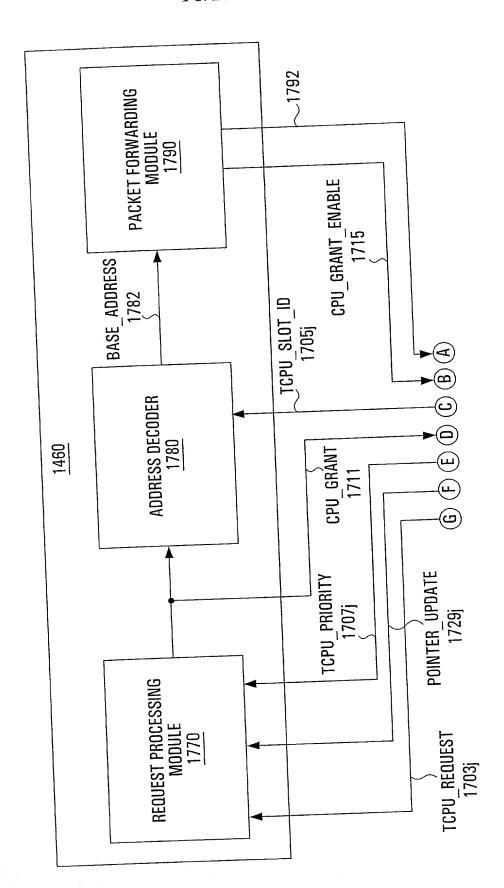
FIG. 15



17/21 210j WRITE ENABLE 518 WRITE ADDRESS 516 1450 506 1450j 1702 PACKET INSERTION MODULE 1704 508_{M^*} 1708 508_{2} 508, CPU_ALMOST_FULL 1408 NEW PACKET 528 OUEUE FULL 526 5 READ ADDRESS 1793j 1714 514_{M*} QUEUE CONTROLLER 1710 ALMOST_FULL 208 514, 5142 1795 UPDATE 529j~ 1712 REQUEST 503 -GRANT 511 POINTER 794 GRANT_ENABLE 515 PRIORITY 1792 SLOT ID 505j MUX 1791 592 ABASE ADDRESS 582 PROCESSING PACKET FORWARDING ADDRESS DECODER MODULE 570 REQUEST MODULE 590 580 260

FIG 17A

FIG. 17B



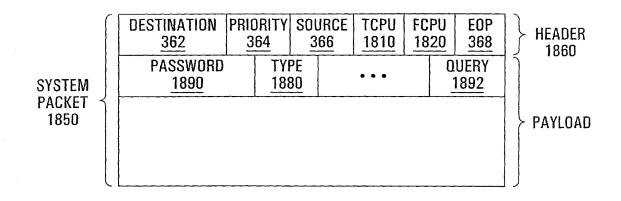


FIG. 18

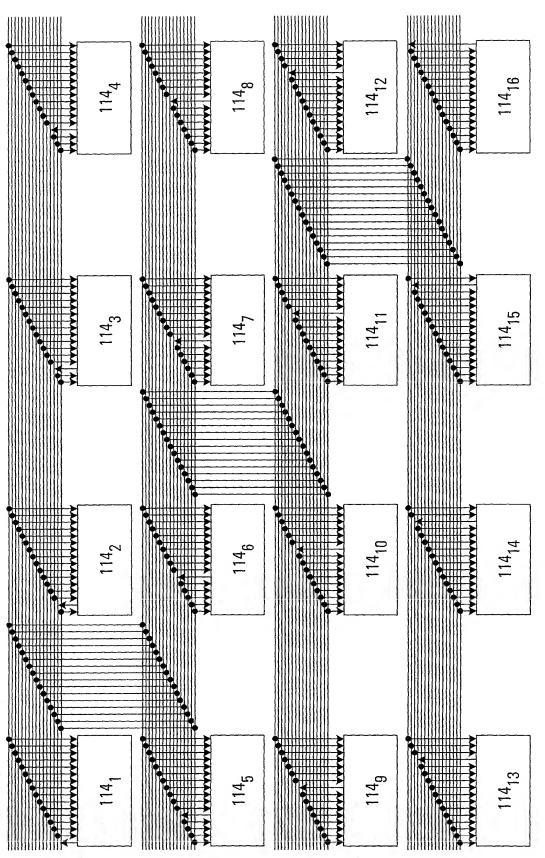


FIG. 19

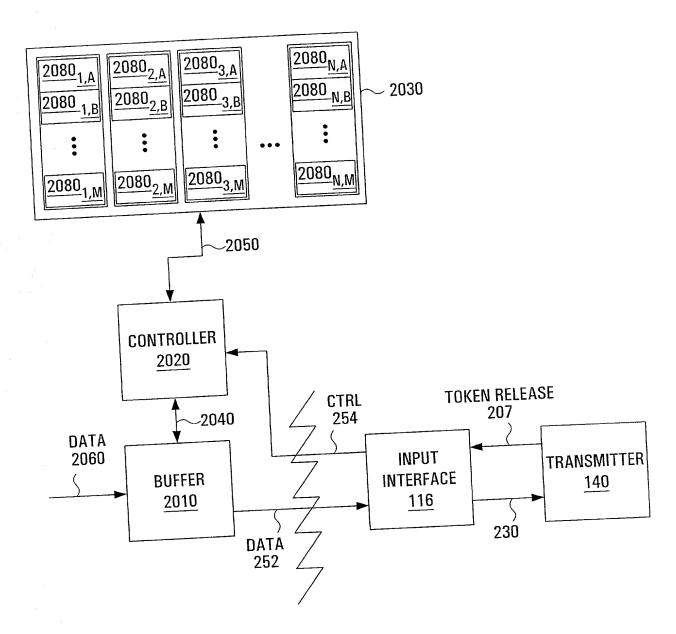


FIG. 20